In the Claims:

Please amend claims 2 and 11, and add new claims 15-19 to appear as in the following listing of claims, which replaces all prior versions.

1. (Canceled)

2. (Currently Amended) The integrated circuit of claim 11, wherein the ~~means for receiving test results comprises a~~ test response analysis unit comprises a multiple input shift register to ~~for~~ compress~~ing~~ the test response vectors into a checksum that can be checked against a reference~~, the integrated circuit further comprising a test control block for controlling the test procedure~~.

3. (Canceled)

4. (Previously Presented) The tester of claim 10, comprising a test response analysis unit arranged to compress test response vectors received from the integrated circuit to be tested.

5. (Previously Presented) The tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time.

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Previously Presented) A tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

11. (Currently Amended) An integrated circuit comprising:

~~means for receiving from an external tester test vectors for testing~~ logic circuitry to be tested using test vectors generated by an external tester;

a test control block to control testing of the logic circuitry; and

a test response and analysis unit to receive test results ~~means for receiving~~ from the logic circuitry ~~test results~~ in response to the test vectors, to produce ~~for producing~~ a compact representation of said test results,[[;]] and to output ~~for outputting~~ said compact representation to the external tester.

12. (Previously Presented) A method of testing logic circuitry of an integrated circuit, comprising:

generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

13. (Previously Presented) The method of claim 12, wherein the integrated circuit includes a test response analysis unit, further comprising:

receiving from the logic circuitry test results in response to the test vectors;

producing a compact representation of said test results; and

outputting said compact representation to the external tester.

14. (Previously Presented) The method of claim 13 wherein said compact presentation includes test vectors applied directly to the external tester to enable fault localization on the logic circuitry.

15. (New) The tester of claim 10, wherein the programmable test vector generator is programmed to generate pseudo-random test vectors and deterministic test vectors for the logic circuitry.

16. (New) The tester of claim 10, wherein the programmable test vector generator is programmed to generate test vectors for the logic circuitry in real time.

17. (New) The method of claim 12, further comprising programming the programmable test vector generator to modify the test vectors based on the logic circuitry to be tested.

18. (New) The method of claim 12, further comprising programming the programmable test vector generator to generate test vectors for the logic circuitry in real time.

19. (New) The method of claim 12, further comprising programming the programmable test vector generator to generate test pseudo-random test vectors and deterministic test vectors for the logic circuitry.